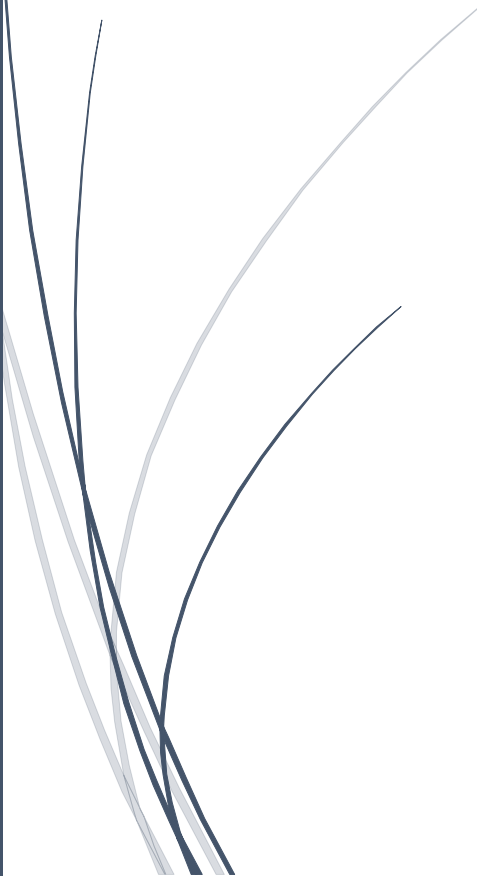


The logo consists of a dark blue vertical bar on the left and a blue arrow pointing right, containing the text "RADemics".

RADemics

FPGA Based Real Time ECG Signal Processing for Smart Health Monitoring Devices

Abstract line art consisting of several thin, curved lines in dark blue and light grey, originating from the bottom left and extending upwards and to the right.

A. Selin Vironicka, Muralidharan J
BISHOP HEBER COLLEGE, KPR INSTITUTE OF
ENGINEERING AND TECHNOLOGY

FPGA Based Real Time ECG Signal Processing for Smart Health Monitoring Devices

¹A. Selin Vironicka, Assistant Professor, Department of Computer Application, Bishop Heber College, Bharathidasan University, Trichy, Tamilnadu, India. mdselin93@gmail.com

²Muralidharan J, Associate Professor, Department of Electronics and Communication Engineering, KPR Institute of Engineering and Technology, Coimbatore, Tamil nadu, India. muralidharanae@gmail.com

Abstract

The integration of real-time electrocardiogram (ECG) signal processing into smart health monitoring devices demands high-performance computing platforms that ensure low latency, high accuracy, and energy efficiency. Field-Programmable Gate Arrays (FPGAs) have emerged as a compelling solution, offering customizable architectures capable of executing complex biomedical signal processing tasks with minimal power consumption. This chapter presents a comprehensive study on FPGA-based QRS detection systems tailored for wearable and portable healthcare applications. Key aspects such as noise suppression, real-time feature extraction, algorithm simplification, and hardware optimization are examined with a focus on achieving robust, low-power, and real-time ECG analysis. A detailed comparison with conventional software-based implementations highlights the advantages of FPGA platforms in terms of processing speed, energy efficiency, and deterministic performance, validation frameworks, benchmarking methodologies, and resource utilization metrics are discussed to guide scalable and clinically viable system development.

Keywords: FPGA, ECG signal processing, QRS detection, real-time systems, low-power architecture, smart health monitoring

Introduction

The rapid advancement of wearable health technologies and the increasing global burden of cardiovascular diseases have created a pressing need for real-time and continuous cardiac monitoring solutions [1]. Electrocardiography (ECG) serves as one of the most vital non-invasive diagnostic tools for identifying heart rhythm abnormalities, arrhythmias, and other critical cardiac conditions. Traditional ECG monitoring systems rely heavily on centralized processing and offline analysis, which introduce latency and limit their suitability for immediate intervention [2]. To overcome these limitations, modern healthcare systems are shifting toward edge-level processing, wherein data acquisition and analysis occur locally on embedded platforms [3]. This approach enables instant response, reduces communication overhead, and improves data privacy, all of which are essential in smart health environments [4]. Among the emerging hardware solutions for edge processing, Field-Programmable Gate Arrays (FPGAs) are gaining prominence due to their configurability, parallelism, and efficiency in executing signal processing tasks with minimal latency and power consumption [5].

Implementing ECG signal processing, particularly QRS detection, on FPGA hardware introduces specific design challenges that differ from traditional software-based implementations [6]. QRS detection involves identifying the most prominent feature in an ECG waveform, which is essential for extracting heart rate, detecting arrhythmias, and evaluating heart rate variability [7]. The accuracy of QRS detection can be severely impacted by motion artifacts, baseline wander, and powerline interference—common occurrences in ambulatory monitoring scenarios. Therefore, the design of a robust signal preprocessing pipeline on FPGA is critical to ensuring signal clarity and enhancing detection reliability [8]. Unlike microcontroller-based systems, FPGAs allow for dedicated hardware resources to be allocated to each signal processing function, enabling highly parallel execution and real-time performance [9]. This parallelism, must be balanced with resource utilization, power consumption, and thermal management to suit the constraints of wearable devices [10].